PRODUCT INFORMATION

ZENI EDA SYSTEM (VLSI BACK-END DESIGN SOFTWARE)

Zeni EDA System Overview:

The **Zeni EDA System** (Hereafter called "Zeni") is a new generation of IC design and development system having user friendly and flexible interface. It is widely compatible with the popular EDA systems and supports numerous standard data conversion formats. Deliberately design functions enable the design masters to save very much time. And powerful localized technique back up has become one of the most prominent highlights. Particularly, some of the products such as layout editor and verification tools are equal to or even better than those of the other EDA Products.

More than 20 years accumulation:

- ✓ In 1988, started to develop 1st generation EDA tools
- ✓ Released Panda in 1992
- ✓ Released Panda2000 in 1997
- ✓ Released Zeni in 2001
- ✓ Released Zeni4 in 2004
- ✓ Released Zeni5 in 2006

Zeni Key Benefits:

- Simple, easy to learn and easy to use
- Consistent with Cadence GUI style and operation mode
- Provides full-Custom, multi-process design
- High performance-price ratio

Compatibility:

- Support importing/exporting schematic data of EDIF 200
- Support importing/exporting layout data of GDSII
- Support process conversion among Cadence technologies

The Zeni EDA System includes the following tools:

ZeniSE: Schematic Editor

Zeni Spice: Aeolus Spice Simulator provides true SPICE accuracy verification solution.

ZeniPDT: Physical Design Tool (includes ZeniIP&R)

ZeniVERI: Layout Verification (DRC/ERC/LVS)

ZeniPE: Parasitic parameter Extraction

ZeniSI: Signal Integrity

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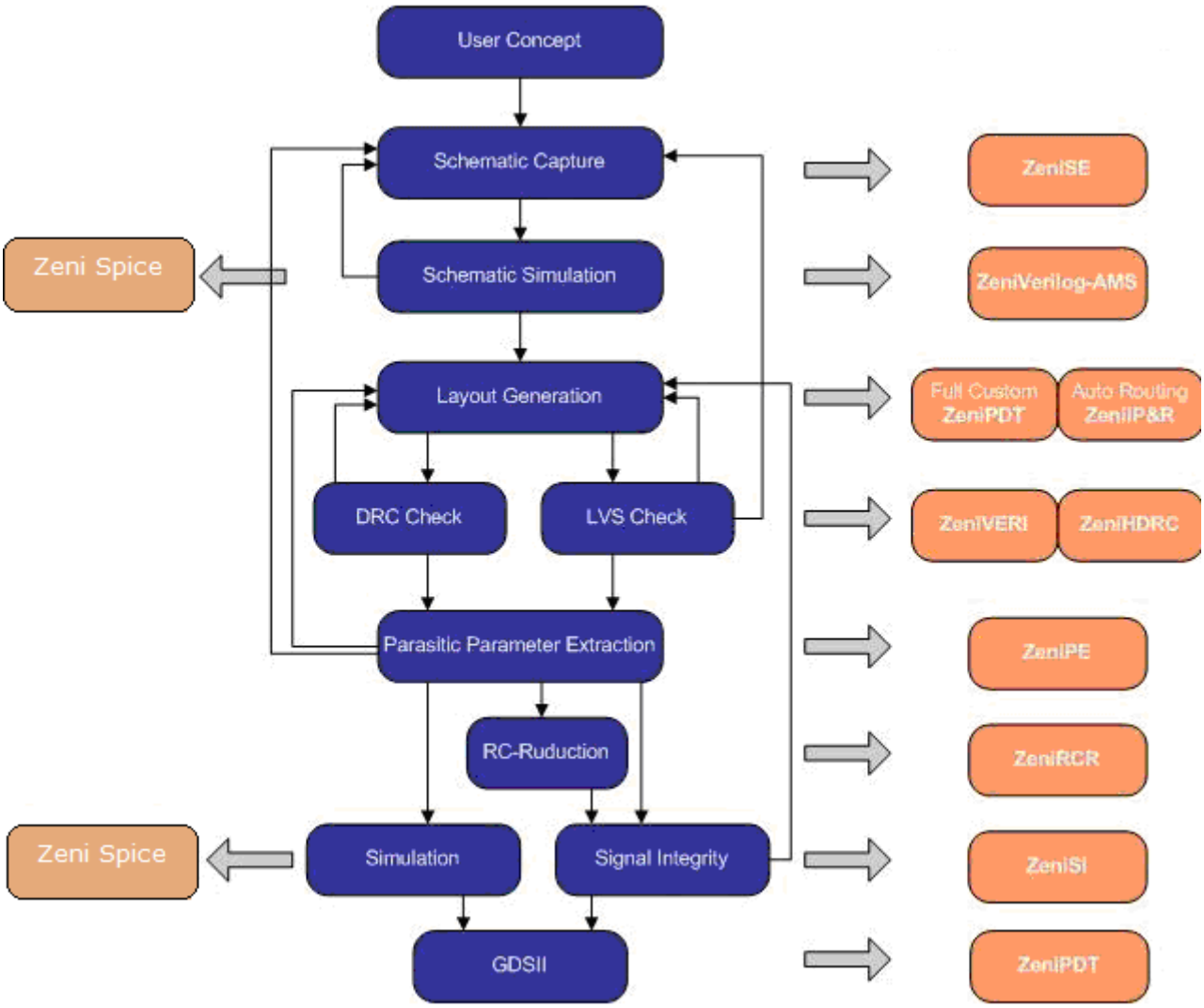
The Complete Solution… (Design Flow)



The Zeni EDA System offers various tools for IC Design Flow, which covers complete VLSI Backend Design Flow. The Zeni framework is popular in because of its ability to interface with external tools. Whereas PC based Tools (Educational tools) suffer from not being able to handle larger industrial strength designs or the detail work like extraction and verification or even providing a path to generating a layout, these tools are limited in functionality and features like post layout extraction with parasitics, which is important before GDS II export. Zeni EDA System has dedicated tools for verification (DRC, LVS, Parasitic Parameter extraction, RCR, Signal integrity).

Similarity to Cadence: Since most custom IC designers use the Cadence DFII environment, using Cadence or an environment similar to Cadence will allow new designers and consultants to come up to speed quickly. Anyone familiar with Cadence will understand how to use Zeni instantly. Virtuoso/Dracula/Calibre lib compatibility, most foundries support Cadence Virtuoso (creation) and Dracula/Calibre's DRC/LVS. Zeni does a good job working or converting these files. EDIF from Cadence works flawlessly with Zeni EDA

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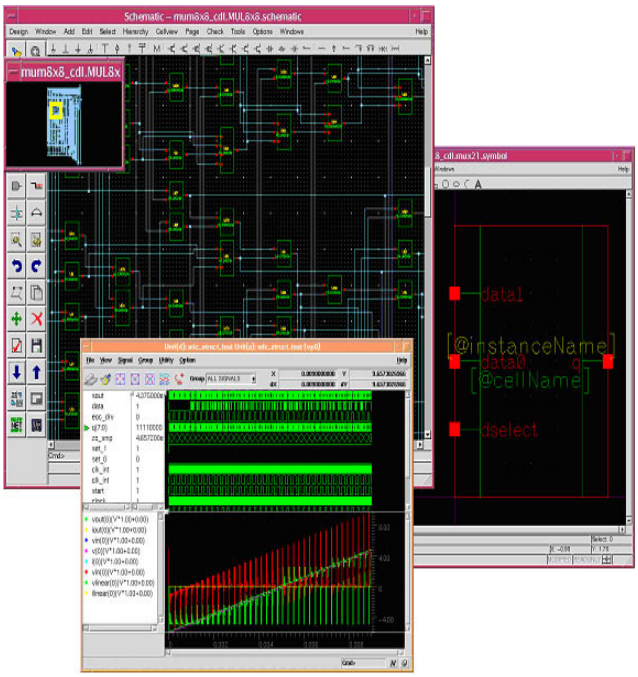
1. Schematic Editor – ZeniSE

Schematic Editor has flexible editing features and it provides a powerful schematic design capability. It supports EDIF import/export and a variety of formats of netlist output, with powerful functions such as a graphical simulation platform, schematic-driven-layout generation, and annotation to back-end tools, etc.



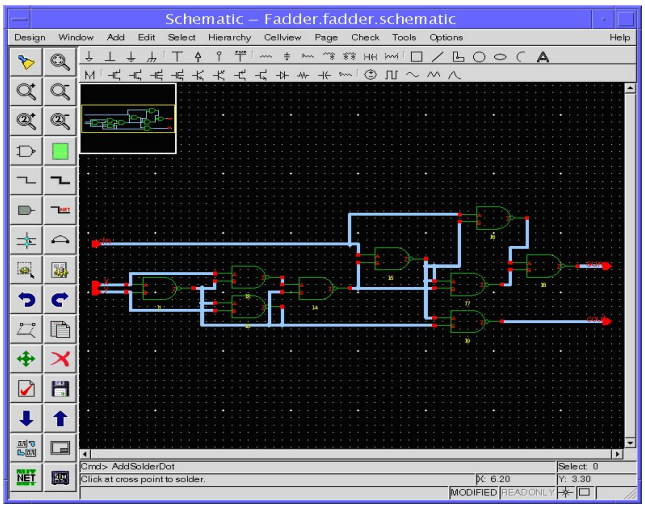
Functions

- **Synchronous multi-window editing, support for world-view**

- **Powerful design capability**
  Hierarchical, multi-page design
  Instantiation component into array
  Connect different networks by name
  Parameter to pass the device properties
  A variety of electrical rule checking options
- **Flexible editing**
  Automatic routing and a variety of ways to connect networks
  Trace and mark signal line
  Hierarchically find/replace components and their properties
  Instantiation component into array
  Custom print border styles
- **A variety of input and output interfaces**
  EDIF standard format import and export
  SPICE, CDL, Spectre, VHDL and Verilog netlist output

Features

- Support Mixed-signal design via view configuration
- Annotation of extracted parasitic parameter results
- Predefined and pre-simulation parasitic parameters
- Annotation and tracing LVS errors
- Automatic Schematic Generation from Netlist
- Extensible graphical SPICE simulation environment
- Node waveform tracing
- Schematic Driven Layout generation



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2. Spice Simulator: Zeni Spice- Aeolus

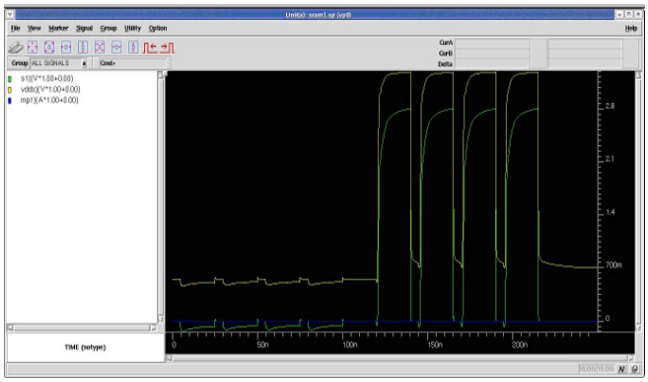
Aeolus is a true SPICE simulator. With advanced parallel simulation algorithms, it delivers accurate simulation with incomparable speed and capacity for analog, mixed-signal designs.. Besides complicated analog circuits, Aeolus is also applicable for mix-signal circuits, critical path analysis and circuit cell library characterization. Aeolus is compatible with popular analog design flows and foundry device models.

- 100% spice accuracy
- Fully compatible with HSPICETM and SPECTRETM format netlists, analysis functions and models
- Industry-leading simulation speed
  - 5~10X faster than traditional SPICE simulator under single thread simulation mode
  - 3~7x additional speedup under parallel simulation mode with 8 CPU cores
- Capable of handling designs with millions of elements, which enables designers to verify the full-chip design of transistor level with SPICE accuracy
- Tightly integrated with ZeniSE™

AEOLOUS Spice simulator runs simulation with highest speed of any other true spice simulators. In serial simulation, AEOLUS is 10X faster than traditional spice simulator. With advanced parallel simulation algorithms, AEOLUS provides 5~7x additional speedup in 8 threads.

Benchmarks

Testcase	Element	MOS	AEOLUS	Traditional SPICE	Speedup
Sram	3.2M	3.2M	6.3 ks	N/A	Infinite
Buffer	500k	500k	984 s	44.6 ks	45
Extrated Block	26k	15k	8.7 s	307 s	35
PLL frequency Synthesizer	540	468	409 s	2620 s	6.4
10-bit ADC	5.2k	5.1k	2.3 ks	21.1 ks	9.3
Charge-pump PLL	236	225	2.6 ks	28.3 ks	11



Features of Aeolus

- Provides true spice accuracy without any device simplification
- Supports millions of transistors on 32-bit platform
- Fully compatible with netlists, commands, device models and waveform in hspice and spectre format
- Supports Verilog-A HDL
- Parallel device evaluation and parallel matrix solver
- Supports both multi-core and distribution simulation
- Unique Newton-Raphson iteration technology which improves performance and stability
- Unique multiple timestep technology which accelerates circuit simulation with different frequencies
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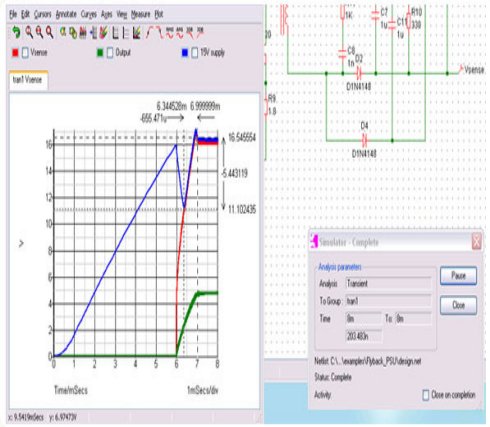

Analysis Types

DC, AC, Tran, OP, PZ, FFT, Monte-Carlo
Multiple parameter sweep

Device Models

- Linear resistor, capacitor, inductor, behavioral resistor, capacitor
- Independent voltage and current source, dependent voltage and current source
- Diode, Bipolar, Bsim3, Bsim4, Bsim4 Soi, Jfet, PSP, EKV3, Bsim3, Bsim4, Bsim4, SOI, PSP, EKV3

- Transmission line, S-parameter

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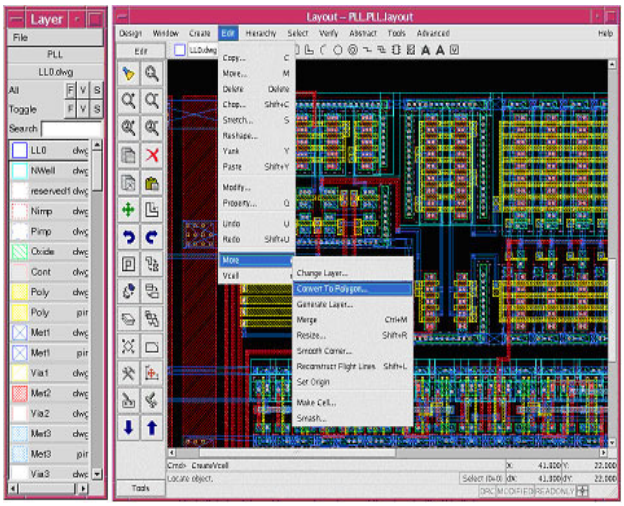
3. Physical Design Tool – ZeniPDT

Zeni Physical Design Tool (ZeniPDT) is a hierarchical, multi-window, full-custom IC layout editing environment. It supports the physical implementation of custom digital, analog and mixed-signal designs at the device, cell, block and full chip levels. It also offers support for physical design debugging and verification by embedded physical verification tools. Furthermore, it can load third-party verification error files and display violations on the layout and schematic.
The Layout tool offers basic creation, customization and data exchanges of parameterized cells (Vcell) between design tools, allowing designers to transfer, maintain and re-parameterize cells in either design system.



Main Functions

- Hierarchical editing for any shaped geometries
- Multiple windows co-editing
- Centralized technology data management
- Capable to handle very large scale layout design
- Supporting industry standard data format like
- GDSII, CIF, LEF and DEF
-
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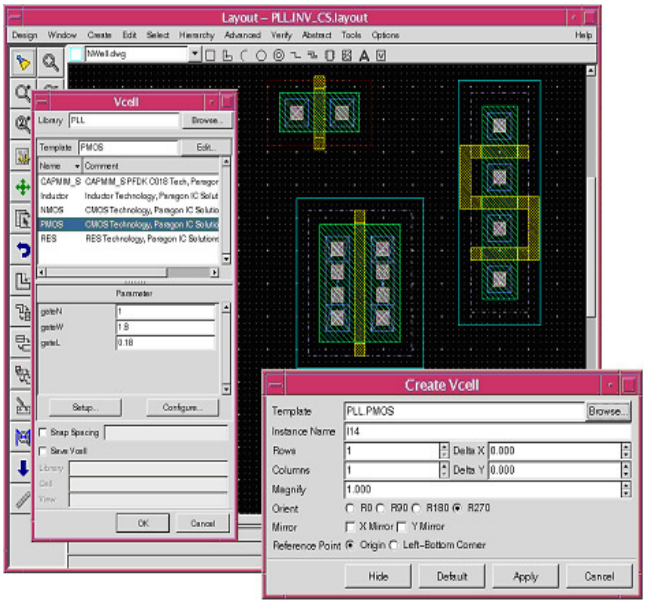
Features

- Automatic memory array generation
- Tracing net and short location
  - Powerful variable cell (VCELL) based on TCL
  - Point-to-point path finder
  - Interactive (real-time) DRC check
  - Abstract view for pin and obstruction creation
  - DRC/LVS error back-annotation for industry popular verification tools



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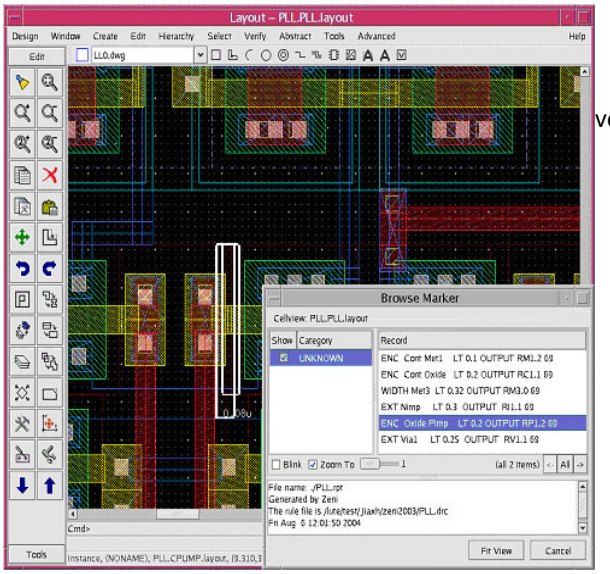
4. ZeniVERI

ZeniVERI is a layout verification tool, “design rule check”(DRC), “electrics rule check”(ERC) and “layout vs. schematic”(LVS) can be performed. It still provides you a graphical LVS debugger tool “LDX”. In ZeniVERI, Errors can be back annotated to ZeniPDT and ZeniSE, which will help you save time while you mend these errors.



Functions

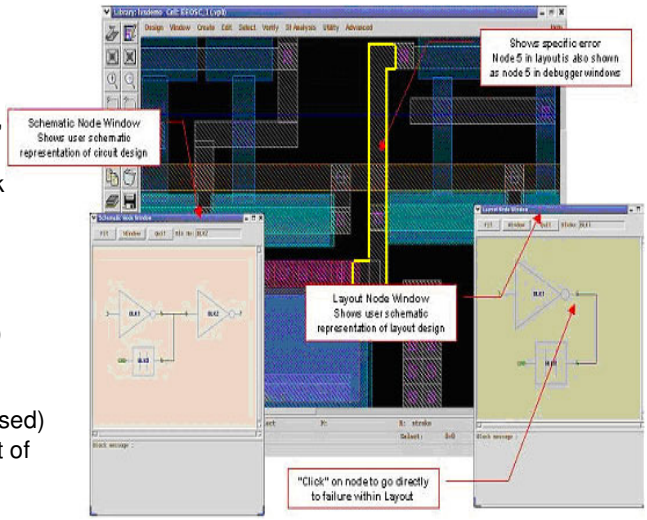
- Perfect solution for physical verification（DRC/ERC/LVS）
- Standard interfaces for design data and technology（ GDSII/CIF/CDL/SPICE/Verilog）
- Directly invoked in ZeniPDT
- Defferent mode to perform verification
- Graphical LVS debugger tool

Application mode

- Online Mode
- Interactive Mode
- Patch Mode

Features

- Fast process verification and accurately back-annotate
- Intuitionistic interface to accelerate modifying errors of DRC, ERC check
- Wieldy LDX debugger tool makes LVS process double quick
- Most Advanced and Efficient Debug Capabilities
- GUI-based Interactivity
- Hierarchical Signal/Short Tracer
- More debug capabilities than any tool in its class (5 modes of DRC, LVS & DRC debugger, trace/signal short)
- LVS Troubleshooting and Debug Capability
- Direct Support of Existing Foundry Verification Decks
- Uses existing foundry decks (Dracula-based and Calibre-based)
- Single Solution - significantly reduces costs for development of multiple decks and support of multiple tools



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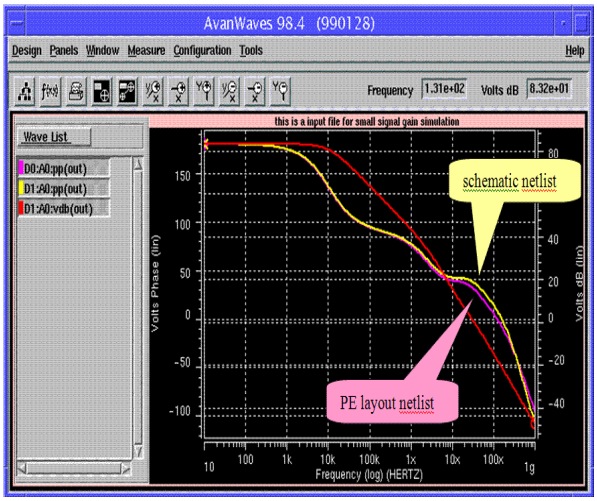
5. Parasitic Extraction – ZeniPE

Parasitic extraction is basically calculation of the parasitic effects in the interconnects of an IC layout: parasitic capacitances, parasitic resistances and parasitic inductances, commonly called parasitic devices, or simply parasitics. Major purposes of parasitic extraction are signal delay calculation, timing analysis, circuit simulation, and signal integrity analysis.

ZeniPE provides accurate and robust capabilities for full chip RC extraction and Signal integrity analysis. The accurate results provide the ability to achieve fast time-to-market by eliminating costly problems through timing analysis, power analysis, critical path/net modeling, and reliability verification. Zeni's PE tool offers the best value on the market today.

Features

- Zeni's PE GUI is flexible and easy-to-use
  - interface with capabilities for controlling full chip and full circuit extraction
  - critical net/node interactive analysis and extraction
- User can choose from various modes and features
  - Quickly modify the PE runset
  - Choose 3 precision modes for C (accuracy vs. speed)
  - Choose 2 precision modes for R (accuracy vs. speed)
  - Coupled or decoupled RC data
  - Choose to extract RC or just C



- PE's speed and accuracy results from a proprietary Quasi 3D field solver and associated algorithm
- Speed and accuracy is enhanced through the use of proprietary source code that only calculates an "RC slice" once and reuses the accurate information for duplicate "slices"
- Accurately extracts 3 dimensional fringing, corner, and cross-coupling effects producing results within 10% of Raphael-NES.
- Proven quasi 3-D numerical field solver and algorithm is correlated with a full 3-D field solver to ensure accurate results at fast speeds
- Creates accurate netlists ready for post extraction and back annotated simulation

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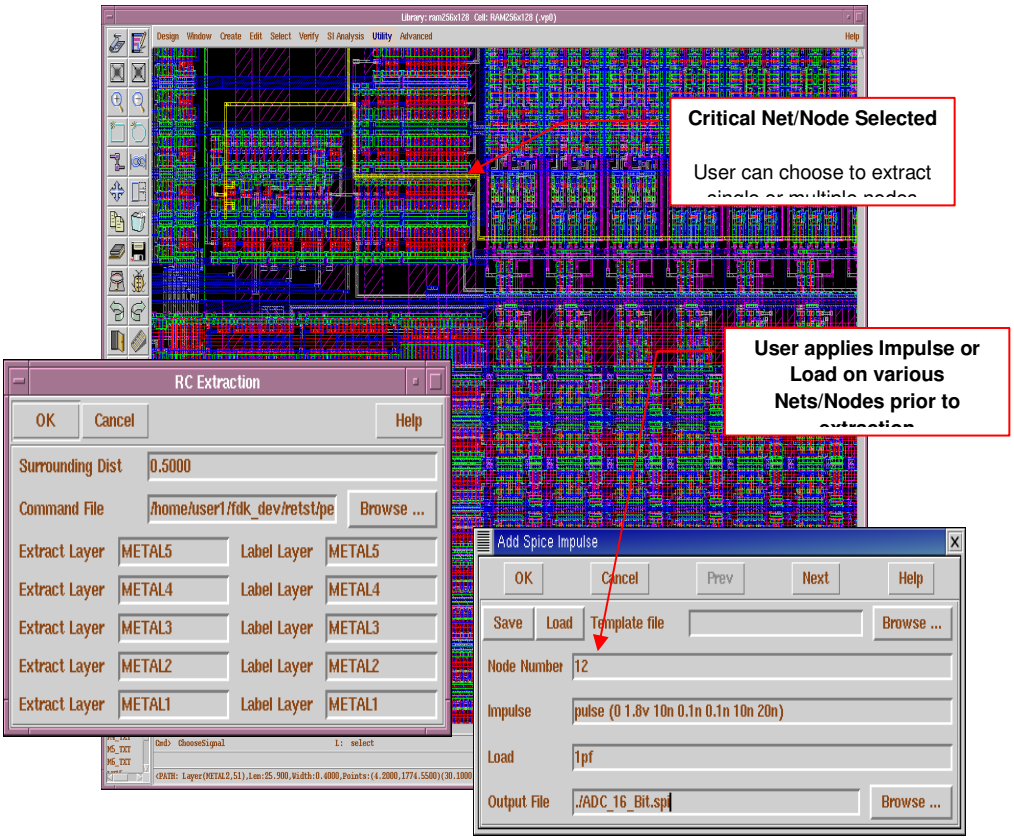
6. Signal Integrity Analysis - ZeniSI

Signal integrity or **SI** is a measure of the quality of an electrical signal. In digital electronics, a stream of binary values is represented by a voltage (or current) waveform. Over short distances and at low bit rates, a simple conductor can transmit this with sufficient fidelity. However, at high bit rates and over longer distances, various effects can degrade the electrical signal to the point where errors occur, and the system or device fails. Signal integrity engineering is the task of analyzing and mitigating these impairments. Signal integrity engineering is an important activity at all levels of electronics Design.

ZeniSI Tool has following features:

- Ability to choose Critical Nets for extraction
- Uses Zeni's PE tool for extraction of critical nets and surrounding parasitic effects
- Ability to place loads and stimuli on multiple nodes prior to extraction
- Creates simulation ready netlist
- Supports measurement of digital bus effects on critical analog layout

Signal Integrity Analysis



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